REMARKS

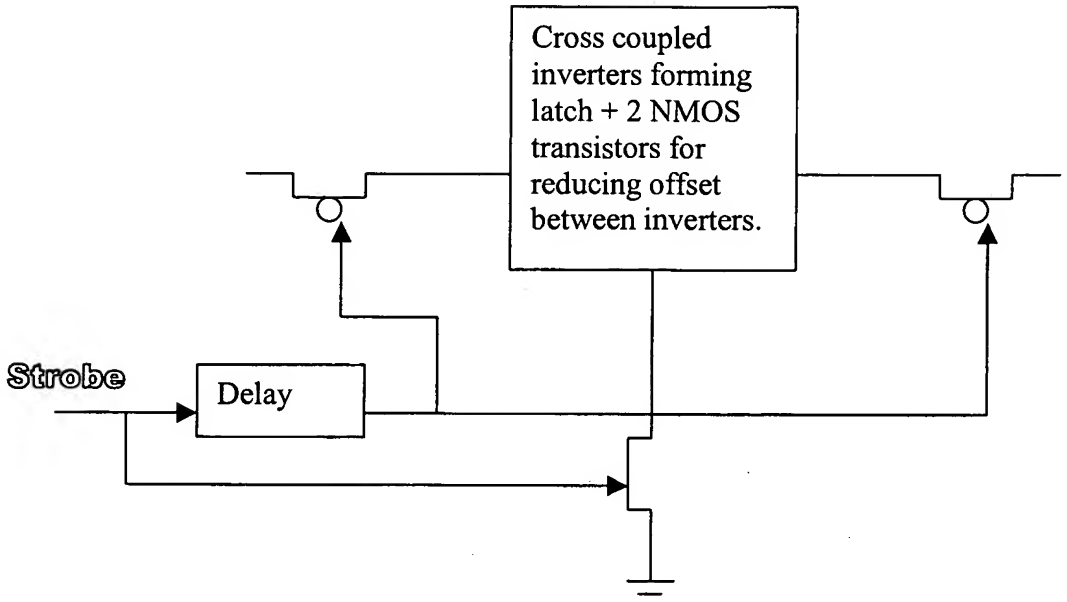
Claims 1-28 are presented for further examination. Claims 1, 2, 7, 9, 10, 12, 13, and 23 have been amended. Claims 26-28 are new.

In the Office Action mailed November 10, 2004, the Examiner rejected claims 1-3, 5-7, 9-18, and 20-25 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,936,905 ("Proebsting"). Claims 4, 8, and 19 were found to be allowable if rewritten into independent form.

Applicants respectfully disagree with the basis for the rejection and request reconsideration and further examination of the claims. The disclosed embodiments of the invention will now be discussed in comparison to the applied reference. Of course, the discussion of the disclosed embodiments and the discussion of the differences between the disclosed embodiments and the subject matter described in the applied reference do not define the scope or interpretation of any of the claims. Rather, such discussed differences merely help the Examiner to appreciate important claim distinctions discussed thereafter.

The disclosed embodiments of the invention are directed generally, to improvements in a sense amplifier circuit. In the disclosed embodiments, a delay is introduced between the connection of supply coupling means to a latch and disconnection of a bit line coupling means to the latch. In addition, two NMOS transistors have been introduced in another embodiment between inverters of a latch and a supply coupling means to reduce the offset between the inverters of the latch. Set forth below is a schematic illustrating the scheme of the present invention:

Our scheme:

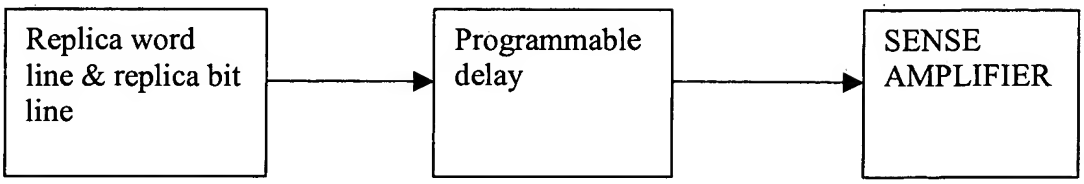


Proebsting, U.S. Patent No. 5,936,905, describes a self-adjusting delay circuit and method for compensating a sense amplifier timing clock. Proebsting's claims are directed to a scheme for accurately generating a strobe signal for a sense amplifier using a dummy word line and a dummy bit line. The dummy word line replicates the actual word line, and the dummy bit line replicates the actual bit line. This enables the strobe signal to track the actual word line and the actual bit line. The strobe signal enables the sense amplifier. In Proebsting's approach, the sense amplifier is only part of the scheme and is known in the art. Proebsting does not claim any improvement within the sense amplifier circuit.

The Examiner states "In Proebsting's scheme Fig: 2, the NMOS transistors (214, 216) are the compensating means for correcting the offset between inverters of the latch." Applicants respectfully submit that this is not correct. In actuality, in Proebsting's scheme the NMOS transistors (214, 216) are the means for connecting the complementary bit lines (IN, INb) to the sense amplifier. In contrast, the present invention utilizes NMOS transistors added between inverters of the latch and the supply coupling means to act as compensating means to reduce the offset between inverters of the latch.

Set forth below is a schematic of Proebsting's scheme:

Proebsting scheme:



In summary, though Proebsting has mentioned a sense amplifier, it is only a part of his scheme of generating a strobe signal for the sense amplifier. Proebsting does not teach or suggest any improvement in the sense amplifier circuit itself. His description and claims are directed to an improved scheme for generating a strobe signal for a sense amplifier.

Turning to the claims, claim 1 is directed to a sense amplifier for a memory array providing increased reliability in sensing small voltage differences that comprises two cross-coupled inverters forming a latch, supply coupling means for selectively connecting the latch to a supply source, bit line coupling means for selectively connecting inputs of each inverter to complement bit lines from the memory array, and delay means for delaying the disconnection of the bit lines from the sense amplifier after the latch has been coupled to a supply source. As discussed above, nowhere does Proebsting teach or suggest the introduction of a delay means between connection of the supply coupling means to the latch and disconnection of the bit line coupling means to the latch. In view of the foregoing, applicants respectfully submit that claim 1 and dependent claims 2-8 are clearly in condition for allowance.

Method claim 9 similarly recites delaying the disconnection of the bit lines from the sense amplifier until a predetermined duration after coupling the latch with the supply source. Applicants respectfully submit claims 9-12 are allowable for the reasons why claim 1 is allowable.

Claims 13-17 recite similar limitations and are also allowable for the reasons why claim 1 is allowable.

Claim 18 recites the introduction of the two NMOS transistors between inverters of the latch and the supply coupling means to reduce the offset between the inverters of the latch. Nowhere does Proebsting teach or suggest any such modification of the sense amplifier circuit.

Applicants respectfully submit that claim 18 as well as dependent claims 19-20 are allowable for these reasons.

Claim 21 is directed to a method for sensing voltage differences that is also allowable for the reasons why method claim 9 is allowable, *i.e.*, the latch circuit is disconnected from the complementary bit lines after a predetermined delay from enabling of the latch circuit.

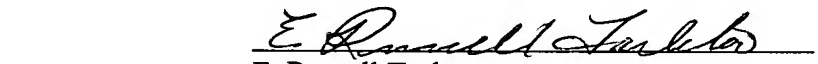
New claims 26-28 are allowable claims 4, 8, and 19 rewritten into independent form. In view of the allowance of independent claims 4, 8, and 19, applicants respectfully submit that new claims 24-26 are also allowable.

In view of the foregoing, applicants submit that all of the claims in this application are clearly in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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